Patent No. 6,020,759 in view of Young U.S. Patent No. 5,933,023.

Applicants' Reply

Claims 1-12 have been rejected under 35 U.S.C. § 103 as being obvious from Heile in view of Young. This rejection is respectfully traversed.

Applicants in a previous Reply to Office Action explained the functions of both (a) applicants' invention, and (b) that which is disclosed by Heile, as background to enable the Examiner to understand the specific differences between the subject matter of Heile and the subject matter of applicants' claims. As part of that explanation, applicants stated that Heile failed to disclose "(3) interconnection resources that are less than fully populated, but (4) are sufficiently populated to allow a particular interconnection conductor to be connected to corresponding conductors in both the read port and the write port."

The Examiner has misread the cited portion of applicants' argument. First, the Examiner appears to believe that applicants' position is, in part, that they invented interconnection resources that are less than fully populated (element "(3)" above). This is not applicants' position. Indeed, the Examiner's prior art for this "element" of applicants' invention is applicants' own statement in the same earlier Reply to Office Action that such interconnection resources were known. The Examiner's position, then, is that even though applicants admitted that the "element" was old, they nevertheless were asserting it as their invention. Applicants would like to lay this illogical position to rest. At no time did applicants

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* (...continued)
However, in view of the Examiner's reliance on a combination of references, the rejection must be considered to be a rejection under Section 103.

believe, or intend to suggest, that they invented less-than-fully populated interconnection resources.

What applicants did invent is a combination that, as explained in the earlier Reply to Office Action, includes "(1) programmable interconnection resources that connect conductors in said groups of interconnection conductors to one another and to said plurality of logic resources, (2) a first programmable interconnection resource for connecting port conductors in said read port ***to a selected one*** of said plurality of groups of interconnection conductors and a second programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said write port ***to said selected one*** of said plurality of groups of interconnection conductors, [where the] (3) interconnection resources ... are less than fully populated, but (4) are sufficiently populated to allow a particular interconnection conductor to be connected to corresponding conductors in both the read port and the write port."

It must be noted, then, that applicants' claimed combination includes not just any less-than-fully populated interconnection resources, but less-than-fully populated interconnection resources with a particular characteristic. Specifically, the less-than-fully populated interconnection resources, while less than fully populated, are sufficiently populated to allow a particular interconnection conductor to be connected to corresponding conductors in both the read port (through one of the less-than-fully populated interconnection resources) and the write port (through another of the less-than-fully populated interconnection resources).

In this context, applicants have defined "corresponding" in the specification. At page 12, lines 22-36, applicants state that

> corresponding read port conductors and write port conductors must be able to be connected to the same ones of conductors 13, 14. For example, if the seventeenth one of write port conductors 23

can be connected to the 103rd, the 156th and the 192nd ones of conductors 13, 14, then the seventeenth one of read port conductors 25 must be able to be connected to at least one of the 103rd, the 156th and the 192nd ones of conductors 13, 14 in order for device 10 to be able to be configured for RAM array 11 to be used as a single-port RAM. This is accomplished in accordance with the invention by arranging the available pattern of connections when constructing the less than fully populated programmable interconnection resources 22, 24 to assure that the necessary connections are available.

Neither Heile nor Young, nor the combination of Heile and Young, shows interconnection resources populated in the manner defined by applicants.

With respect to Heile, applicants have previously shown why Heile alone neither shows nor suggests the claimed invention. The Examiner apparently agrees, having added Young to the rejection (although the Examiner repeats verbatim his earlier explanation of how Heile alone anticipates the claims). However, Young does not make up what is missing from Heile, in neither showing nor suggesting the claimed invention.

The Examiner relies on a passage in Young that describes how one of the logic blocks could generate a clock signal that can be routed onto a general interconnect line and from there to a clock line that can feed both the A and B clocks of the Young RAM. This, with respect, has nothing to do with the element of applicants' claims that requires that the less-than-fully populated interconnection resources be sufficiently populated to allow a particular interconnection conductor to be connected to <u>corresponding</u> conductors in both the read port and the write port.

First, the A and B ports in Young are not the read and write ports. Young shows two dual-port memories, designated A and B, that can be used separately or as a single larger memory. Thus, in Young, there are an A read port, an A write port and an A clock (CKA), and there are a B read port, a B write port and a B clock (CKB). So the fact that a clock signal can reach both CKA and CKB is

irrelevant to applicants' invention, because those inputs belong to completely separate memories and do not "correspond" to each other within the meaning of applicants' claims.

"Corresponding" is defined in the specification as set forth above. For Young to show that defined feature of the invention would mean, for example, that in Young some single conductor such as, e.g., L0-3, would have to be guaranteed access through two separate less-than-fully populated programmable interconnection resources, to, e.g., both DIA7 (a write port conductor in the A RAM) and DOA7 (the corresponding read port conductor). Similarly, another conductor, such as, e.g., L3-7, would have to be guaranteed access through the two separate less-than-fully populated programmable interconnection resources, to, e.g., both DIB2 (a write port conductor in the B RAM) and DOB2 (the corresponding read port conductor). Similar access would have to be guaranteed between a respective individual interconnection conductor and a respective pair of "corresponding" read and write conductors in both the A and B RAMs. However, Young does not include such a teaching. Indeed, applicants cannot find a single pair of corresponding read port and write port conductors in the drawings of Young for which the required relationship is true.*

Moreover, applicants respectfully submit that the combination of Heile and Young is improper. The Examiner

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* Applicants first respectfully point out that their identification in this discussion of particular conductors from the Young specification is completely arbitrary and is made for illustrative purposes only.

Second, applicants point out that while their specification shows a dual-port memory where the read and write ports have separate address inputs but share data input/output lines, Young shows dual-port memories where the read and write ports share address inputs and have separate data output and input lines, respectively. However, applicants do not believe that this distinction is significant, as they believe their claims are generic to both embodiments.

has not established any suggestion or motivation in either of the references for making the combination, and it is axiomatic that motivation or suggestion is required.

Nor does any such motivation or suggestion exist. Heile and Young are directed to distinctly different problems. Heile shows a programmable logic device of the look-up table type that also includes RAM that can be configured to emulate product term ("p-term") type logic. Young, on the other hand, shows a programmable logic device in which RAM can be configured in different sizes, shapes, heights and widths. There is no reason why someone of ordinary skill in the art who was looking to emulate p-term logic in RAM would look to a reference that taught how to change the size of RAM. There is equally no reason why someone of ordinary skill in the art who was looking to change the size of RAM would look to a reference that taught how to emulate p-term logic in RAM.

Indeed, Heile actually teaches away from the claimed invention. Heile states that "when [the RAM] is used in p-term mode, ... only reading is affected" (column 4, lines 1-2), and that "the write port is available during p-term operation" (column 7, line 33). As the Examiner put it in the Advisory Action in the parent application, the interconnections in Heile "allow[] independent writing and reading or writing without interfering with reading." This is ***precisely the opposite*** of the claimed invention, where each read port conductor may be coupled through the interconnect resources to a corresponding write port conductor, thereby ***preventing*** independent writing or reading operations, as is characteristic in a single-port memory.

For these reasons, applicants respectfully submit that the claimed invention is patentable.

Conclusion

For the reasons set forth above, applicants respectfully submit that this application is in condition

for allowance. Reconsideration and prompt allowance of this application are respectfully requested.

Respectfully submitted,

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